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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,509	07/30/2001	Katsuhiko Hieda	04329.2613	8843

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/916,509	HIEDA, KATSUHIKO	
	Examiner	Art Unit	
	Thao X Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 24-45* is/are pending in the application.

4a) Of the above claim(s) *3-21 and 24-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 35-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 35-37 and 39-45 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 5,567,962 to Miyawaki et al.

Regarding to claims 1, Miyawaki discloses a semiconductor device comprising a convex semiconductor layer 1016/1021, fig 17, provided on a semiconductor substrate 1012, a source region 1030, column 10 line 32, and a drain region 1017, column 9 line 59, provided in the convex semiconductor layer 1016/1021, a semiconductor region 1016 (P), fig. 14, having a impurity concentration higher than that of the channel region 1021 (P^-), fig. 14, column 13 line 9-12, provided between the source and drain regions (S/D), the semiconductor region 1016 provided between the semiconductor substrate and the source region, between the semiconductor substrate and the drain region, and between the semiconductor substrate and the channel region, respectively, fig. 14, a gate electrode 1023, column 10 line 11 having side-wall gate portion column 10 line 11, provided over a side a side surface of the convex semiconductor layer, the gate electrode applying an electric field to the channel region 1021 region and the semiconductor region 1016 via a gate insulator 1022 in fig. 19 column 13 line 45, and the side-wall gate portion

being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region, fig. 14.

Regarding to claim 2, Miyawaki discloses a semiconductor device comprising a convex semiconductor layer 1016/1021, fig 17, provided on a semiconductor substrate 1012, a source region 1030, column 10 line 32, and a drain region 1017, column 9 line 59, provided in the convex semiconductor layer 1016/1021, a semiconductor region 1016 (P), having a impurity concentration higher than that of the channel region 1021 (P^-), column 13 line 9-12, provided between the source and drain regions (S/D), the semiconductor region 1016 provided between the semiconductor substrate and the source region, between the semiconductor substrate and the drain region, and between the semiconductor substrate and the channel region, respectively, fig. 14, a gate electrode 1023, column 10 line 11 having side-wall gate portion 1023, column 6 line 53-60, provided over a side a side surface of the convex semiconductor layer, the gate electrode applying an electric field effect to the channel region 1021 region via a gate insulator 122, fig. 19 column 13 line 45, and the side-wall gate portion being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region and a side-wall insulating film 1086 provided on a side surface of the gate electrode and the side surface of the convex semiconductor layer, fig. 25.

Regarding to claim 35, Miyawaki discloses a semiconductor device wherein a distance between the S/D regions becomes longer toward a lower portion from the upper portion of the convex semiconductor layer, fig. 24.

Regarding to claim 36, Miyawaki discloses a semiconductor device wherein the impurity concentration of the S/D region becomes lower toward a lower portion from an upper portion of the convex semiconductor layer, column 15 line 26. This is also known as LDD structure

Regarding to claim 37, Miyawaki discloses a semiconductor device wherein the sidewall gate portion is formed to portion under the S/D region along the side surface of the convex semiconductor layer, fig. 25

Regarding to claim 39, Miyawaki discloses a semiconductor device wherein a width of the convex semiconductor layer is smaller than the depth of the S/D region. The depth of S/D regions 1030/1017, fig. 11-14, would be corresponding to d_1 and $d_3<d_1$, column 10 line 55.

Regarding to claim 40, 41, 42, Miyawaki discloses a semiconductor device wherein at least one of the S/D regions includes at least two kinds of diffusion layers 1030 and 1085, a high and low concentration N^+ and N^-, having a dense impurity concentration diffusion layer, and the convex semiconductor is electrically connected to the conductive substrate, fig 25

Regarding to claim 43, Miyawaki discloses a semiconductor device comprising a gate insulating film 1022 is made of a Si oxide, column 10, line 9.

Regarding to claim 44, 45, Miyawaki discloses a semiconductor device wherein a position of a deepest portion of the gate electrode is deeper that a position of the deepest portion of the S/D region, fig. 10, 11, 12, and 13.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,567,962 to Miyawaki et al.

Regarding to claim 38, Miyawaki does not disclose a semiconductor device wherein a width of the convex semiconductor layer is smaller than 0.2 μm.

But Miyawaki discloses the width d_3 of the channel, column 6 line 63 and column13 line 49-51. This width would be corresponding to the width of the convex semiconductor layer. Accordingly, it would have been obvious to one of ordinary skill in art to use or combine (teaching of second reference) in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Response to Arguments

4. Applicant's arguments filed on 12/10/03 have been fully considered but they are not persuasive. The Applicant argues on the ground that the thickness of the gate insulator of the instant application is being constant while Miyawaki does not discloses a constant gate insulator, in page 21 last paragraph or fig. 8A. The Examiner respectfully disagrees because gate insulator 1022 in fig. 12 of Miyawaki does show the top portion is being constant from one end to other. Claim in a pending application should be given their broadest reasonable interpretation. In re

Pearson, 494F.ed 1399, 181 USPQ 641 (CCPA 1974). In this case, the rejected claim of the instant application does not exclusively require the gate insulator must be constant on the entire surface of the convex semiconductor layer, thus such constant thickness of layer 1022 of Miyawaki would read the claim language. Furthermore, although the claim are interpreted in light of the specification, limitation from the specification are not read into the claim, see In re Van Geuns, 988 F.22d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Also, it is proper to use the specification to interpret what the applicant meant by a word or phase recited in the claim. However, it is not proper to read the limitations appearing in the specification into the claim when these limitations are not recited in the claim; *Intervet America Inc. v. Kee-Vet Lab. Inc*, 887 F.2d 1050, 1053, 12 USPQ2d 1474, 1476 (Fed. Cir. 1989).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
08 Mar. 2004